ABSTRACT OF THE DISCLOSURE

An apparatus and method of synthesizing an output clock signal from a source clock signal. The clock synthesizer includes a phase generator, a phase selector, a phase interpolator, and control circuitry for controlling the phase selector/interpolator. The phase generator receives a high speed clock, and generates P phases of the source clock to define P phase sectors. The phase selector selects respective pairs of phases such that each pair bounds a respective phase sector. The phase interpolator introduces at least one phase of the source clock between each pair of phases to provide Q phases of the source clock within each sector. The phase interpolator uses the phases of the source clock to produce lagging (leading) phase shifts of 360/P(Q-1) degrees, thereby generating the output clock having a stepped up or stepped down frequency.

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ATTORNEY DOCKET NO. TI-34685 (UNITI-169XX)
WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313